

Local Oscillator Sub-systems for Array Receivers in the 1-3 THz Range

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ABSTRACT

Recent results from the Heterodyne Instrument for the Far-Infrared (HIFI) on the Herschel Space Telescope have confirmed the usefulness of high resolution spectroscopic data for a better understanding of our Universe. This paper will explore the current status of tunable local oscillator sources with emphasis on building a multi-pixel LO subsystem for the scientifically important CII line around 1908 GHz. Recent results have shown that over 50 microwatts of output power at 1.9 THz are possible with an optimized single pixel LO chain. These power levels are now sufficient to pump array receivers in this frequency range. Further power enhancement can be obtained by cooling the chain to 120 K or by utilizing in-phase power combining technology.

Keywords: Schottky diodes, frequency multipliers, local oscillators, heterodyne receivers

1. INTRODUCTION

Submillimeter-wave spectrometry is a proven flight technique that is essential for NASA's unique goals, such as atmospheric remote sensing [1], study of cosmic water profiles [2, 3], comet characterization [4], and investigation of cosmological phenomena with radio telescopes [5]. Recent results obtained from HIFI have shown spectacular emission and absorption spectra with unprecedented resolution and have demonstrated the feasibility and utility of using spectrally resolved C+ fine-structure spectral line emission ([CII]) at 1.9 THz as a tracer for components making up the interstellar medium [6,7,8]. Beyond space-based instrumentation, terahertz imaging for homeland security has also been getting much attention with recent demonstration of sub-cm resolution imaging at 670 GHz [9]. One of the most challenging aspects of terahertz technology is the lack of compact, reliable, efficient, and broadband sources in the terahertz range. Sources are required for a variety of applications, either as transmitters or as local oscillators (LO) for heterodyne detectors. Post-HIFI progress has been made in different areas that open new possibilities for future heterodyne receivers that can continue the observations of the star forming regions of our galaxy as well as extra-galactic sources in the 1-3 THz range. The main effort is now focused on producing a LO sub-system to enable high resolution multi-pixel spectroscopy beyond 1 THz. In particular, the CII line around 1.908 THz is of special interest to the scientific community and a multi-pixel system is strongly needed to make large scale maps.

2. A NEW SINGLE-PIXEL 1.9 THZ LO SOURCE WITH STATE-OF-THE-ART PERFORMANCE

The HIFI Band 6b LO source produced around 2 μ W of power at 1.9 THz (with 100 mW of input power at W-band) under room temperature (300K). We have now developed a new generation of multiplier chips that using the same multiplier scheme of $x2 \times x3$ can now produce substantially more output power. While producing 100 mW at W-band was challenging for HIFI, nowadays 150-200 mW can be easily achieved cascading 3 or 4 GaAs pHEMT MMIC amplifiers. In addition, the design procedures of high frequency multipliers are now much better understood and the optimization of the semiconductor devices characteristics is performed with a much better understanding. For example, power-handling is one of the main limitations to frequency multiplier, which occurs when the input signal to the multiplier becomes large enough to drive the diodes into reverse breakdown. The anode area, the number of anodes per chip, and doping levels have been optimized to have a good trade of between power-handling and performance. This has allowed us to measure conversion efficiencies very close to the theoretical limits predicted for Schottky diode based frequency multipliers. Obviously, the improvements on the fabrication process has also played a major role for the post-Herschel generation of frequency multiplied sources; the utilization of the membrane technology for multipliers has

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reduced considerably the circuit losses at very high frequencies, and the precise definition of the submicron Schottky anodes using electron beam lithography has boosted the performance of these devices beyond 1 THz.

As a result, we have recently demonstrated a new 1.9 THz chain able to provide 30-60 μ W at room-temperature in the 1.9 THz frequency range when pumped with 100-200 mW around 105-115 GHz, see Fig.1. This represents an improvement of a factor of 20 with regards to the 1.9 THz LO chain onboard HIFI. At temperatures around 120K, the performance is expected to improve further by 3 dB or so. It is important to remark again that this multiplied chain, depicted in Fig.1 (right) is a direct evolution of the IIFI/Herschel chain with optimized single-chip frequency multiplier stages with no power-combining of any kind. The performance as a function of frequency of this 1.9 THz LO chain is shown in Fig. 2. Assuming that 2-5 μ W are necessary to adequately pump a single-pixel HEB receiver, this power level is already sufficient to pump an array of HEB mixers (at least 4 pixels with a health contingency margin to account for waveguide and coupling losses) in the 1900 GHz range to map the ionized carbon line in our galaxy. A number of approaches can be used to pump the array receiver. The single horn output of the LO can be multiplexed via a Fourier grating [10] or a waveguide based power splitter can be utilized to split the power into multiple pixels.

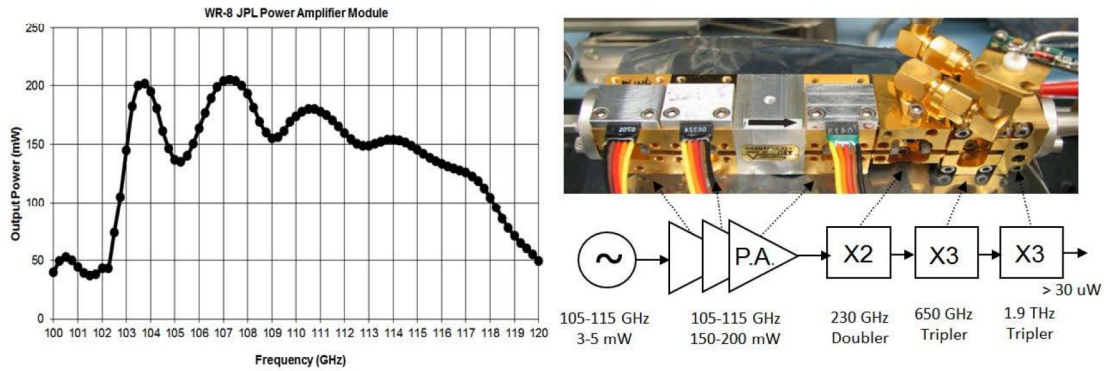


Figure 1: Single-pixel LO sub-system for the next generation of solid state array receivers for the CII line.

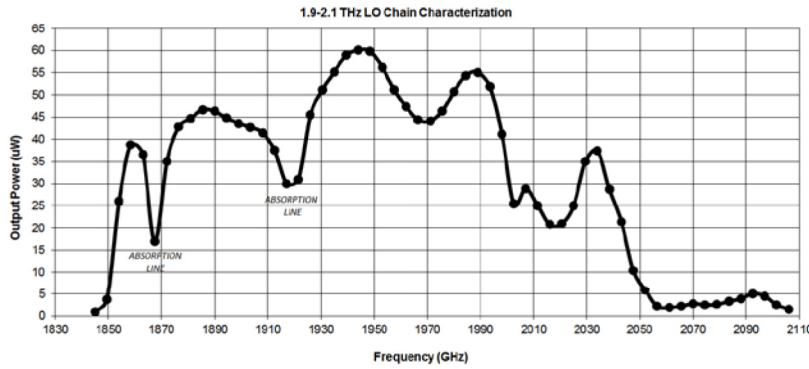


Figure 2: Performance of the new JPL 1.9 THz LO sub-system at room temperature. The last stage tripler is bias-less and the measurement is made without any attempt to correct for water absorption.

The chain in Figure 2 is driven by a six-anode balanced 230 GHz doubler (see Fig. 3). This chip is constructed on a relatively thick substrate to provide appropriate thermal environment. The diodes are made on $1 \times 10^{17} \text{ cm}^{-3}$ doped epilayer to enhance power handling capability and reduce risk of breakdown. The doubler is optimized for an input power of ~ 150 mW but still performs well for input power levels around 200 mW. The doubler chip is shown in Fig. 3 (left) and the measured performance when pumped with the amplifier (of Fig.1) is presented in Fig. 3 (right).

The second-stage multiplier in the chain (Fig. 4) is a bias-able 650 GHz tripler which has been specifically designed to be pumped by the previous 230 GHz frequency doubler. As for the 230 GHz doubler, this design considers a epitaxial layer doping of around $1 \times 10^{17} \text{ cm}^{-3}$. It was optimized for an input power of around 25-30 mW and features only 2-anodes in a balanced configuration on a thin GaAs membrane. The efficiency saturates at around 35 mW input power but the tripler still performs well up to 40 mW of input power without showing any thermal degradation.

The last-stage 1.9 THz tripler (see Fig. 5) consists of a bias-less 2-anode balanced structure on a thin GaAs membrane. The doping is $>3 \times 10^{17} \text{ cm}^{-3}$ to mitigate the impact of electron velocity saturation. The design was optimized for 1 mW input power. However, as can be seen in Fig. 5 (right), the tripler exhibits very good efficiency for input power levels within the 0.5 mW to 2 mW range. According to Fig. 5 (right) an output power of around 10-15 μW is possible with only 0.4-0.5 mW of input power, which is more than enough to pump a single-pixel receiver based on HEB mixers. The results presented above demonstrate that an optimized 1.9 THz LO chain can produce enough output power to sufficiently pump a 4-pixel receiver.

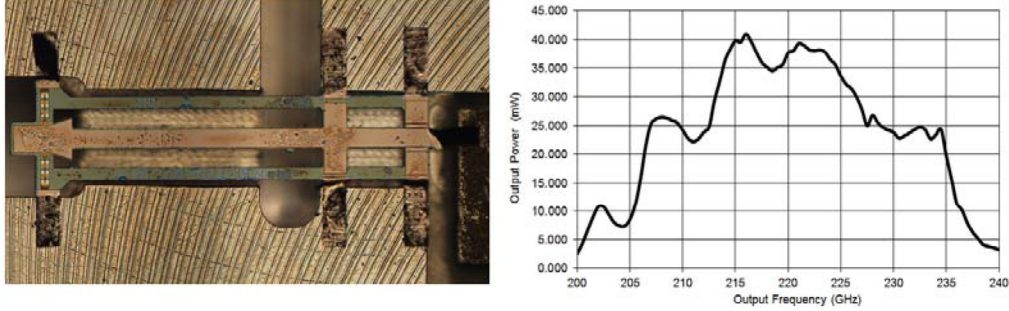


Figure 3: First-stage of the JPL 1.9 THz LO sub-system: 230 GHz doubler. Chip photo (left) and performance (right)

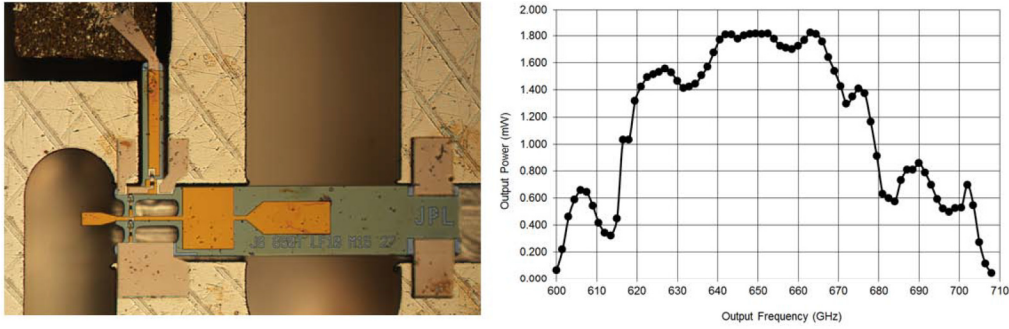


Figure 4: Second-stage of the JPL 1.9 THz LO sub-system: 650 GHz tripler. Chip photo (left) and performance (right)

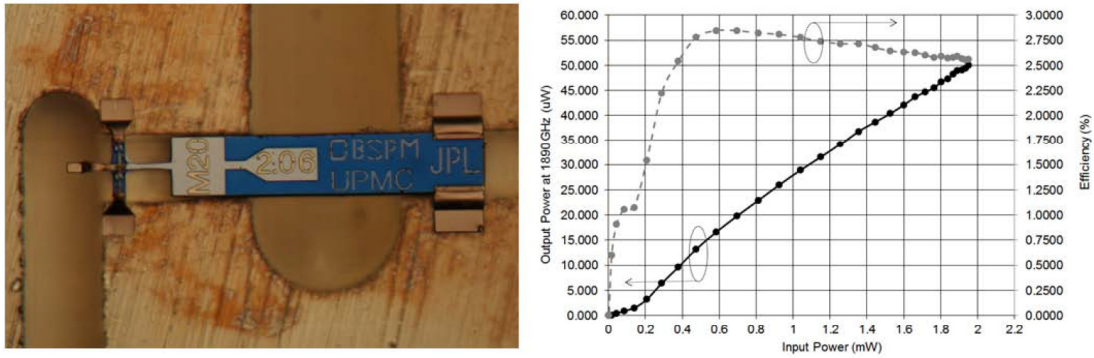


Figure 5: Third-stage of the JPL 1.9 THz LO sub-system: 1.9 THz tripler. Chip photo (left) and performance (right)

3. TOWARDS 1.9 THZ LO SUB-SYSTEMS FOR ARRAY RECEIVERS

For array receivers one will have to start with higher power drivers in the W-band. Utilization of waveguide based power-combiners as well as the introduction of W-band GaN power amplifiers can provide the necessary boost in power. A 4-way power combining scheme with InP based p-HEMT devices has already been demonstrated [11] with output peak power of 0.72 Watts and a 3-dB bandwidth of 92-110 GHz. Similarly, the rapid advancement in GaN based power amplifier technology has made it possible to surpass the 1W limit at W-band. Recent results reported in [12] have shown

that a single GaN - MMIC can be expected to provide power output in the range of 500-750 mW. Furthermore, by power combining 4 chips, power in excess of 3 W has been measured. Similarly, power combining in a rat-race structure has demonstrated power levels in excess of 5 W [13]. The combination of being broadband and having a fairly flat output power profile at these frequencies now makes it possible to utilize this technology as the driving source for high power frequency multiplier chains.

The large amount of available power at W-band now puts the onus on the multiplier designer to successfully harness this power. A number of approaches have been identified to achieve this goal. For a given multiplier design, as the input power is increased, the multiplier will either experience thermal heating or reverse breakdown, both of which will result in catastrophic failure. To improve the thermal handling of multiplier chips, an approach based on utilizing diamond substrates has been previously reported [14]. However, chip thickness or substrate thickness and number of anodes per chip can only be increased up to a limit. In order to avoid unwanted waveguide modes, both of these design parameters are eventually constrained. Increasing power handling capability beyond this point requires novel approaches such as sandwiching dual chips, as suggested in [15]. Another simple approach that has been suggested before and demonstrated is to power combine multiplier circuits in a waveguide based circuit [16]. This approach offers a number of advantages. It is a straightforward concept and does not require any new technology development at the chip level; in fact, existing chips can be utilized. The power combining and dividing functionality is accomplished in the waveguide, allowing for a low-loss transmission media. Moreover, this approach provides an easily scalable design, both in frequency as well as in power. Traditional designs such as the Y-junction and the 90-degree hybrid couplers have been utilized for this approach. A two-chip in-phase power-combined frequency tripler working around 300 GHz was first demonstrated in [17] and has now become an important tool for developing multi-pixel LO subsystems at terahertz frequencies.

Using these ideas, we have designed a 4-pixel LO sub-system at 1.9 THz. This is similar to the LO chain described in the previous section with one main difference. The output power from the second stage tripler will be split and two 1.9 THz tripler chips will be used. Output from each of the 1.9 THz triplers will be divided via a simple Y-junction. A schematic of the last stage tripler block is shown in Fig. 6. Thus, a total of four output beams will be generated from this configuration. The expected output power per pixel is a strong function of drive power and is shown in Fig. 7.

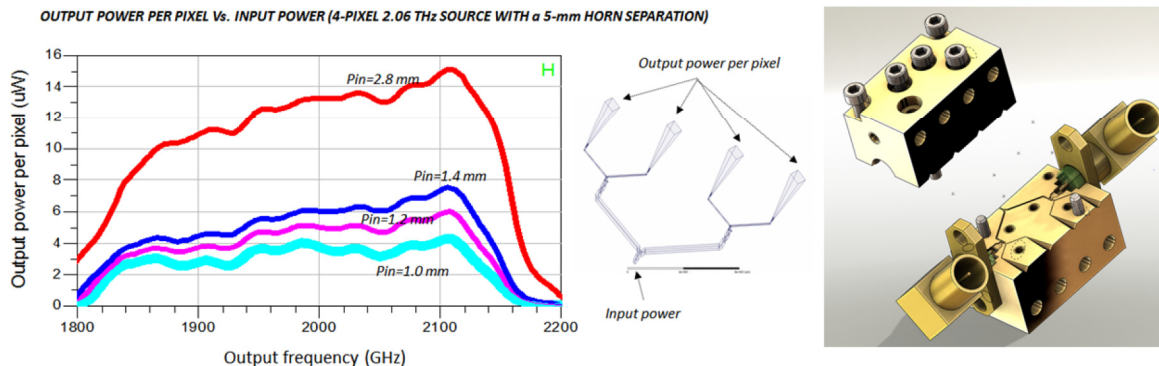


Figure 6: Expected performance from a 4-pixel LO sub-system as a function of the input drive power is shown on the left. Block schematic is shown on the right. Two 1.9THz tripler chips will be used to generate four output beams.

Ultimately, and taking advantage of the > 1 Watt power available at W-band and the power-combining techniques described before, our goal is to extend to a 16-pixel LO sub-system at 1.9 THz with at least 5 μ W output power per output. There are a number of ways for achieving this goal. Two options are shown in Fig. 7. The option on the left utilizes the topology that has been discussed in this paper. For a 16-pixel receiver a total of 16 multiplier chips will be required. One slight drawback of this approach is that not all of the 16 outputs can be controlled independently since each final stage tripler pumps two HEB mixers. A second option is shown in Fig. 7 (right). The first stage doubler will be a quad chip design with relatively thick substrate material. The diamond substrate material described in [10] will be utilized and should allow this circuit to be pumped with close to 1 W of input power. It is expected that this circuit with 4-chips will produce around 150 mW of output power around 212 GHz. This in turn will be used to pump the 2-anode 650 GHz triplers. Each of these triplers is expected to produce around 2 mW of output power at 636 GHz, which will then be used to pump four final stage triplers. This scheme will require a total of 32 multiplier chips but will allow for independent power control on each pixel. A more eloquent solution of using on-chip power combining has also been proposed that can significantly reduce the number of chips up to a factor of 4 [18].

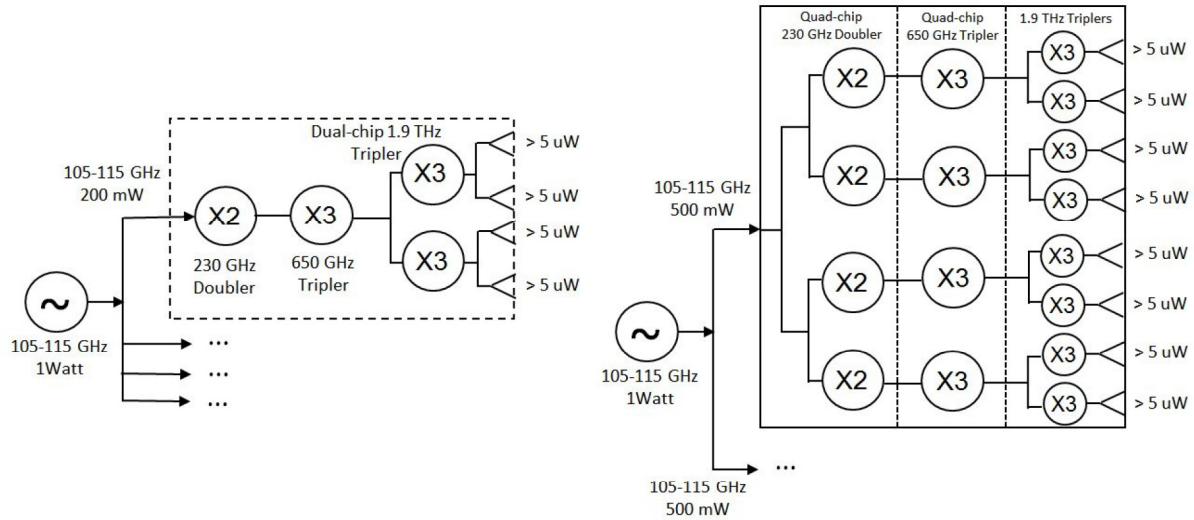


Figure 7: Two possible schemes for generating a 16-pixel LO sub-system at 1.9 THz. The scheme on the left utilizes fewer multiplier chips while the scheme on the right allows for power control of each individual pixel.

4. A 1.9 THZ LOCAL OSCILLATOR CHAIN WITH CONTROL OF OUTPUT POWER

The LO scheme used on Band 7 of HIFI utilizes a non-biased tripler as the final stage (similar to the one shown in Fig. 2). HEB devices are sensitive to LO power and thus for array receivers it could be important to be able to adjust the LO power incident on each pixel. A bias-able 1.9 THz tripler has been designed and fabricated. This allows one to easily adjust the bias of the final stage tripler to control the output LO power from the LO sub-system. Initial tests of this chip confirm that the bias can be used to control the output power from the peak to almost zero as shown in Fig. 7.

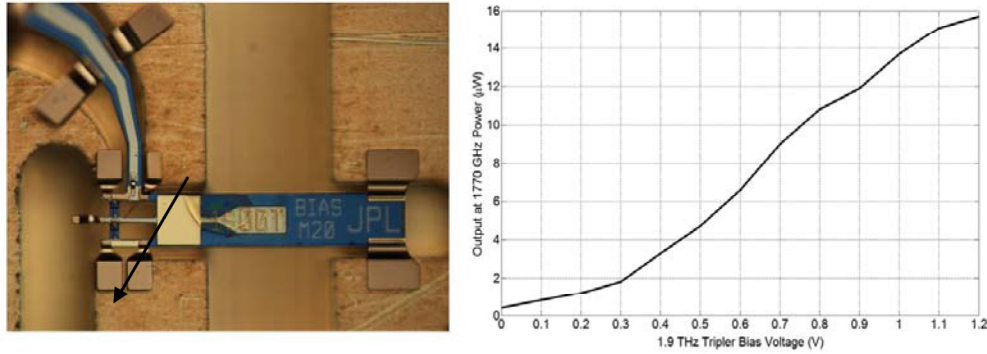


Figure 7: A 1.9 THz tripler chip with bias is shown on the left. The plot on the right shows the output power at 1770 GHz as a function of bias on the 1.9 THz tripler.

5. CONCLUSION

GaAs Schottky diode based multiplied sources continue to advance and provide a well established broadband technology for future array receivers. More than 50 microwatts of output power around 1.9 THz has now been demonstrated and even more power can be obtained by cooling or utilizing simple waveguide based power combining technologies. A 16-pixel LO sub-system is being designed and fabricated.

6. ACKNOWLEDGEMENT

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